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SUBMISSION TYPE: **Information Disclosure Statement**
APPLICATION NUMBER: **09687048**
FIRST NAMED INVENTOR: **Kuri-shi Lee**
TITLE OF INVENTION: **LEADFRAME AND SEMICONDUCTOR PACKAGE WITH IMPROVED SOLDER JOINT STRENGTH**
ATTORNEY DOCKET NUMBER: **AMKOR-052A**

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fee-transmittal	e-feetra.xsl 15388 Bytes
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Docket Number: AMKOR-052A

Title: LEADFRAME AND SEMICONDUCTOR PACKAGE WITH IMPROVED SOLDER JOINT STRENGTH

Client: Amkor Technology, Inc.

Attachments: IDS Electronic Form

By signing below, I authorize the electronic submission of the above-identified Information Disclosure Statement. I have reviewed the document and authorize a member of the support staff to affix an electronic signature on my behalf.

Mark B. Garred

3/17/03
Date

34,823
Registration No.

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TITLE: Leadframe and semiconductor package with improved solder joint strength

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TRANSMITTAL FORM

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Application Number	09/687,048
Filing Date	10/13/2000
First Named Inventor	Tae Heon Lee
Group Art Unit	2814
Examiner Name	Nguyen, Dilinh P.
Attorney Docket Number	AMKOR-052A

ENCLOSURES *(check all that apply)*

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- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
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Stylesheet Version: 1.0

Submission Type: Information Disclosure Statement

Application Number: 09/687,048

Attorney Docket Number: AMKOR-052A

LEADFRAME AND SEMICONDUCTOR PACKAGE WITH IMPROVED SOLDER JOINT STRENGTH

First Named Inventor: Kuri-shi Tae Heon Lee

SUBMITTED BY

Name:	Mark B. Garred
Registration Number:	34,823
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Subtotal For Additional Fees: $ 180

MANUFACTURE OF SEMICONDUCTOR DEVICE

Patent Number: JP10256240
Publication date: 1998-09-25
Inventor(s): FUKAZAWA MASANAGA;; KADOMURA SHINGO;; FUKUDA
Applicant(s): SONY CORP
Requested Patent: ☐ JP10256240
Application JP19970158570 19970616
Priority Number(s):
IPC Classification: H01L21/3065; H01L21/768
EC Classification:
Equivalents:

Abstract

PROBLEM TO BE SOLVED: To form a connection hole in an interlayer insulating film by a dry etching process, using not only a general composition etching gas but also an etching gas containing no fluorocarbon-loosed gas.
SOLUTION: This method for manufacturing a semiconductor device includes a step of forming a connection hole 14 in an inter-layer insulating film by a dry etching process using an etching gas. In this case, a film 12 having a low dielectric constant is an insulating film which is made of a compound, having SiF or CF couplings in a chemical structural formula. Specifically, the compound may be SiOF, cyclic fluororesin siloxane copolymer or polyfluoroaryl ether. When such an insulating film employed, active species of F- or fluoroacrbon- boased moleules emitted from inside of the connection hole 24 of the inter-layer insulating film can cause an etching rate of the insulating film inside the hole 14 to be increased.

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] the layer insulation film which consists of a compound which has SiF combination or CF combination in a chemical structure formula by the dry etching using etching gas -- connection -- the manufacture method of the semiconductor device characterized by having the process which forms a hole
[Claim 2] The compound which has SiF combination or CF combination in a chemical structure formula is the manufacture method of the semiconductor device according to claim 1 characterized by the ranges of specific inductive capacity being 1-4.
[Claim 3] the compound which has SiF combination or CF combination in a chemical structure formula -- under etching -- connection of a layer insulation film -- a hole -- the active species of the molecule of F emitted from inside, or a fluorocarbon system -- connection -- a hole -- the manufacture method of the semiconductor device according to claim 1 characterized by including F beyond the grade which can be made to accelerate etching of an inner insulator layer

* NOTICES *

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] the connection formed in the layer insulation film according to the example of this invention -- it is the outline cross section showing a hole
[Drawing 2] It is the outline cross section showing the structure of the sample used for the example of this invention.
[Drawing 3] the connection which tried to form in the layer insulation film used for comparison with the example of this invention -- it is the outline cross section showing a hole
[Description of Notations]
10 Si Substrate and 11 SiO2 Layer and 12 Low Dielectric Constant Film and 13 Photoresist and 14 Connection -- Hole

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[Translation done.]